UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,130	12/31/2001	Jaideep Dastidar	H052617.1150US0	1080

7590 06/28/2005

IP ADMINISTRATION, HEWLETT-PACKARD COMPANY
LEGAL DEPARTMENT, MS 35
P. O. BOX 272400
FORT COLLINS, CO 80527-2400

EXAMINER	
VO, TIM T	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,130	DASTIDAR ET AL.	
	Examiner	Art Unit	
	Tim T. Vo	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/12/02* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

This application has been examined. Claims 1-44 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless --

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-44 are rejected under 35 U.S.C. § **102(e)** as being anticipated by Bashford patent number 6,629,179.

As for claims 1, 19, 36 and 40, Bashford teaches a device for implementing an inter-queue ordering mechanism between different queues of an interconnect of a computer system, comprising: a first circular queue (see figure 4, posted write register 404); a second circular queue (see figure 4, circular queue 408), the first and second circular queues adapted to have an ordering dependency between them (see figures 6, 8 and column 7 line 62 to column 8 line 22 and column 8 lines 39-53, wherein the posted write register 404 includes 16 registers 602-632 and each registers is in sequential order from low to high. Further, figure 8 discloses the circular queue includes 16 registers 802-832 and each register is also in sequential order from low to high), wherein entries in the

second circular queue are not allowed to pass entries in the first circular queue (see figure 4, 408, 404, wherein the data flow from circular queue 408 does not flow into the posted write registers 404); a first counter (see figure 4, posted write tracking circuitry 412 and column 8 lines 11-14, wherein the posted write tracking circuitry 412 for tracking registers in the posted write register 404); and a second counter (see figure 8, circular queue 408 and column 7 lines 3-6 and column 9 lines 5-8, wherein the circular queue keeps track of the order of the interrupt bits as they received from the interrupt entry logic circuitry and also the circular queue keeps tracks of the registers 802-832), the first and the second counters adapted to increment whenever an entry is enqueued to or dequeued from the first circular queue, respectively (see figure 4, posted write tracking circuitry 412, circular queue 408 and column 8 lines 39-55, wherein an incoming interrupt bit number is stored in the circular queue, the circular queue 408 increments the incoming interrupt register 836 to point to the next register in the circular chain of register 802-832).

As for claims 2, 23, Bashford teaches wherein the entry in the second circular queue cannot be dequeued before the entry that was placed earlier in the first circular queue is dequeued (see figure 7).

As for claims 3, 24-25, Bashford teaches wherein the entry in the second circular queue cannot be dequeued before the entry that was placed earlier in the first circular queue is dequeued and then acknowledged as having been completed (see figures 5, 7, 9-10).

As for claims 4, 26 Bashford teaches wherein the dependency ensures that one of the first and second circular queues can proceed with an interconnect transaction as long as the second circular queue entries are not allowed to pass older entries of the first circular queue (see figure 4).

As for claim 5, 27, Bashford teaches wherein the first and second circular queues are comprised in a peripheral component interconnect (PCI) system (see column 4 lines 65-67).

As for claims 6, 28, Bashford teaches wherein the first and second circular queues are comprised in an order enforcement mechanism (see figures 6, 8).

As for claims 7, 33, 38-39, Bashford teaches wherein the first counter rolls over to zero only once before the second counter rolls over to zero (see posted write tracking circuitry 412 and circular queue 408).

As for claims 8-10, 37, 44, Bashford teaches wherein the first and the second counters roll over to zero after reaching respective maximum values (see figure 8 and column 9 lines 5-8).

As for claims 11-12, 29-30, Bashford teaches wherein the first and second circular

queues are incorporated in a North Bridge of the computer system (see figure 1-2, 112, 202).

As for claims 13-15, 20-22, 41-43, 45, Bashford teaches wherein the first and second circular queues comprise first-in-first-out (FIFO) memory (see figures 6, 8).

As for claims 16-17, 31-32, Bashford teaches further comprising ack bits in the first circular queue for maintaining the ordering dependency (see figure 6, B0-B15 and column 8 lines 1-6).

As for claims 18, 34, Bashford teaches further comprising other circular queues, wherein the second circular queue has a dependency on the other circular queues such that an entry in the second circular queue cannot be dequeued unless requirements for dequeuing that entry are met with respect to every queue that the second circular queue depends on (see figures 5, 7 and 9-10).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim T. Vo whose telephone number is 571-272-3642. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

6/24/05

Tim T. Vo
Primary Examiner
Art Unit 2112